REMARKS

Claims 1-18 stand rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al.

Claims 1 and 12 have been cancelled. Claims 2, 8, and 13 dependent from claim 1 and 12 have been rewritten in independent form including all limitations of cancelled base claims 1 and 12.

It is well settled that the Examiner bears the initial burden of establishing a ***prima facie*** basis to deny patentability to a claimed invention under any statutory provision. ***In re Oetiker***, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). Anticipation under 35 U.S.C. § 102 requires the disclosure in a single reference of each element of a claimed invention. ***Minnesota Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.***, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 102, it is incumbent upon the Examiner to point out specifically wherein an applied reference discloses each feature of the claimed invention. ***In re Rijckaert***, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); ***Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.***, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984).

It is respectfully submitted that the Examiner did not discharge that burden with respect to claims 2, 8 and 13. In particular, the Office Action did not address limitations of these claims.

Hence, the Examiner has failed to establish a *prima facie* case of anticipation with respect to independent claims 2, 8 and 13.

In addition, it is respectfully submitted that Wu et al. does not disclose the subject matter of these claims. In particular, the reference does not disclose the scheduler configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry for receiving the data blocks

from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, as claim 2 requires.

Further, the reference does not disclose the logic circuitry that comprises ingress rules logic for receiving the data block to check whether the corresponding data packets are received with an error, as claim 8 recites.

Also, the reference does not disclose that a data queue representing each of the receive ports is assigned with at least one of the time slots, as claim 12 requires. By contrast, Wu teaches that one of the cells of each source with the identified highest priority is assigned to a time slot.

Moreover, it is respectfully submitted that the reference does not disclose limitations of dependent claims 3-7, 9-11, and 14-18. In particular, Wu et al does not teach that:

- each of the plurality of the queuing devices is assigned with at least one of the time slots in each scheduling cycle (claim 3);

- the scheduler is configured to allocate a first time slot assigned to a first queuing device to a second queuing device if no request for a time slot is received from the first queuing device (claim 4);

- the second queuing device is assigned with a second time slot following the first time slot (claim 5);

- the scheduler is configured to allocate the first time slot to a third queuing device if no request for a time slot is received from the second queuing device (claim 6);

- the third queuing device is assigned with a third time slot following the second time slot (claim 7);

- the logic circuitry further comprises source address lookup logic for comparing a source address of the data packets with a preset source address (claim 9);

- the logic circuitry further comprises destination address lookup logic for comparing a destination address of the data packets with a preset destination address (claim 10);

- the logic circuitry further comprises egress rules logic for producing a port vector identifying the at least one selected transmit port (claim 11);

- a first time slot assigned to a first data queue is allocated to the first data queue if the first data queue contains data to be processed (claim 14);

- the first time slot is allocated to a second data queue if the first data queue does not contain data to be processed (claim 15);

- the second data queue is assigned with a second time slot following the first time slot (claim 16);

- the first time slot is allocated to a third data queue if the first and second data queues do not contain data to be processed (claim 17); and

- the third data queue is assigned with a third time slot following the second time slot claim 18).

The Examiner has failed to address these limitations.

Hence, the Examiner's rejection of claims 2-11, 13-18 under 35 U.S.C. 102 is improper and should be withdrawn.

In view of the foregoing, and in summary, claims 2-11, 13-18 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

Entry of the amendment under 37 CFR § 1.116 is respectfully requested because the amendment is limited to canceling claims 1 and 12. In accordance with 37 CFR § 1.116(b), such an amendment may be made after a final rejection.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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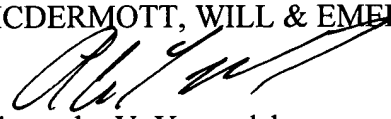

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 2, 8 and 13 were amended as follows:

2. (Amended) A multiport data communication system for switching data packets between ports, the data communication system comprising:

a plurality of receive ports for receiving data packets,

a decision making engine responsive to the received data packets for controlling transmission of the received data packets to at least one selected transmit port,

the decision making engine including:

a plurality of queuing devices corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports,

logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and

a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports [The system of claim 1],

wherein the scheduler is configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry.

8. (Amended) A multiport data communication system for switching data packets between ports, the data communication system comprising:

a plurality of receive ports for receiving data packets,

a decision making engine responsive to the received data packets for controlling transmission of the received data packets to at least one selected transmit port,

the decision making engine including:

a plurality of queuing devices corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports,

logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and

a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports [The system of claim 1],

wherein the logic circuitry comprises ingress rules logic for receiving the data block to check whether the corresponding data packets are received with an error.

13. (Amended) In a communication system having a plurality of receive ports, at least one transmit port, and a decision making engine for controlling data forwarding between the receive port and the at least one transmit port, a method of data processing comprising the steps of:

placing data blocks representing received data packets in a plurality of data queues corresponding to the plurality of the receive ports,

transferring the data queues in successive time slots to logic circuitry for determining the at least one transmit port, and

dynamically allocating the time slots to the data queues in accordance with data traffic at the corresponding receive ports [The method of claim 12],

wherein a data queue representing each of the receive ports is assigned with at least one of the time slots.